ABSTRACT

An approach is disclosed herein to facilitate evaluating integrated circuit (IC) chips. A set of critical paths are determined for a design associated with the IC chip, at least some of which critical paths are based on timing characteristics for the design (*e.g.*, timing margin or slack). Multiple sets of test patterns are generated for the set of critical paths based on desired performance criteria. One or more of the plurality of sets of test patterns can be applied to the IC chip to provide corresponding test data that can be utilized to evaluate chip performance and/or improve the chip yield for the IC design.